Express Mail Label No.

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
TI-25833.1
Total Pages in this Submission
24

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

OPTIMIZED CIRCUIT DESIGN LAYOUT FOR HIGH PERFORMANCE BALL GRID ARRAY PACKAGES

and invented by:

WILLIAM B. STEARNS
NOZAR HASSANZADEH

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☒ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: **09/250,641**

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having **15** pages and including the following:
   - a. ☒ Descriptive Title of the Invention
   - b. ☒ Cross References to Related Applications *(if applicable)*
   - c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   - d. ☐ Reference to Microfiche Appendix *(if applicable)*
   - e. ☒ Background of the Invention
   - f. ☒ Brief Summary of the Invention
   - g. ☒ Brief Description of the Drawings *(if drawings filed)*
   - h. ☒ Detailed Description
   - i. ☒ Claim(s) as Classified Below
   - j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☐ Formal Number of Sheets _____
   b. ☒ Informal Number of Sheets 5
4. ☒ Oath or Declaration
   a. ☐ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☒ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☒ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☒ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☐ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
12. ☒ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☐ Certificate of Mailing
    ☐ First Class ☐ Express Mail *(Specify Label No.):* _____

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Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	8	- 20 =	0	x $18.00	$0.00
Indep. Claims	1	- 3 =	0	x $78.00	$0.00
Multiple Dependent Claims (check if applicable) ☐					$0.00
				BASIC FEE	$690.00
OTHER FEE *(specify purpose)* _____					$0.00
				TOTAL FILING FEE	$690.00

☐ A check in the amount of to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **20-0668** as described below. A duplicate copy of this sheet is enclosed.

- ☒ Charge the amount of **$690.00** as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Signature

Jay M. cantor
Reg. No. 19906
(202) 639-7713

Dated:

cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

WILLIAM P. STEARNS ET AL.

Serial No. 09/250,641 (TI-25833.1)

Filed Herewith

For: OPTIMIZED CIRCUIT DESIGN LAYOUT FOR HIGH PERFORMANCE BALL GRID ARRAY PACKAGES

Art Unit

Examiner

Commissioner for Patents
Washington, D. C. 20231

Sir:

PRELIMINARY AMENDMENT

Prior to the first Office action, please cancel claims 9 to 18, the claims elected in the parent application.

Action and allowance are respectfully requested.

Respectfully submitted,

Jay M. Cantor
Reg. No. 19906
(202) 639-7713

OPTIMIZED CIRCUIT DESIGN LAYOUT FOR HIGH PERFORMANCE BALL GRID ARRAY PACKAGES

CROSS REFERENCE TO RELATED APPLICATIONS

This application is related to provisional application Serial No. 60/046,062 (TI-22215), the contents of which are incorporated herein by reference and is a division of Serial No. 09/250,641, filed February 16, 1999 and priority claimed therein.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

This invention relates to a method of laying out traces on a substrate and the layout for connection of a semiconductor chip to a printed wiring board and the like.

BRIEF DESCRIPTION OF THE PRIOR ART

Semiconductor integrated circuits are formed in semiconductor chips which contain the electrical circuits. Bond pads are generally disposed on the chip with the chip being mounted within a package and the bond pads being connected by wires to lead frame fingers or the like

which extend externally of the chip. The package, after fabrication, is generally secured to a printed wiring board with the lead frame fingers or the like connected to bonding regions on the printed wiring board. The package as well as the electrically conductive members which transfer the signals from the chip to the printed wiring board add to the undesirable loads (i.e., inductances, noise, crosstalk, etc.) which the chip may see with the magnitude of these undesirable loads increasing with increasing chip operating frequency.

A typical package may include a substrate having a cavity which contains a chip within the depression. Bond wires couple bond pads on the chip to individual copper traces on the substrate, the copper traces each extending to an electrically conductive aperture or via which extends through the substrate to an electrically conductive ball pad and a solder ball. The vias and ball pads are formed in a matrix array having plural rows and columns of vias which are located adjacent one or more of the sides defining the depression. Adjacent vias and ball pad centers in a row or a column are spaced apart from each other by a distance defined herein as a "ball pitch", this distance being the dimension from the center of one via or ball pad to the center of the adjacent via or ball pad in the same row or in the same column. The "ball pitch" between all adjacent vias or ball pads in the same row or in the same column is the same. The solder ball is soldered to a pad on a printed wiring board in standard manner as discussed in the above noted copending application to make the connection from the chip to the printed wiring board pad.

The copper traces as well as the bond wires, electrically conductive regions in the vias and surrounding wiring and packaging add additional circuitry to the electrical circuit which bring to the circuit additional resistances, inductances and capacitances. The layout of the circuitry and

especially the layout of the traces materially affects the performance of the chip, this being particularly material in the case of differential wiring pairs wherein pairs of wires carry the same or similar signals but are out of phase with each other. It is therefore apparent that a layout is highly desirable which minimizes the above noted problems of the prior art.

SUMMARY OF THE INVENTION

In accordance with the present invention, the above described problems of the prior art are minimized.

Briefly, the path traversed by each trace of each differential wiring pair is adjusted to have a pitch or distance therebetween substantially equal to or less than a ball pitch as defined hereinabove, to be parallel to each for the maximum possible distance, to each be as close as possible to the same length and to have the same cross-sectional geometry to the closest extent possible. In other words, it is a requirement that the parallel positioning of the trace portion of each differential wiring pair be maximized to the greatest possible extent and that the trace lengths be equalized to the greatest possible extent. The quality of the differential pairs is dependent upon each of (1) the degree of parallelism, (2) equality of length and (3) substantial identity of geometry and spacing between the cross-sections of the two traces forming the differential pair. It is also necessary that each trace of the differential pair be equally spaced from the ground plane, if present, and be tailored to provide maximal performance with respect to the ground plane. The geometry of design is set up to match odd/even mode circuit impedance. Accordingly, the dielectric constant of the substrate separating the signal plane from the ground plane can be controlled to control the impedance in the signal lines as is well known. The geometric relationship between the width, separation, thickness and distance from the ground plane of the conductors also affects the impedance of the conductors.

In the present state of the art, it is possible to provide at most two signal traces between a pair of adjacent columns at minimum ball pitch. In order to meet the above criteria, it has been

found that the above described maximization is obtained, with reference to FIGURE 4, by connecting pairs in the manner 1-2, 1-2 and 3-3. This means that, given three adjacent columns 0, 1, 2 and three rows of vias 1, 2, 3 or connection locations in those columns, a first pair of traces will be connected to rows 1 and 2 of a column 1 with the trace connected to row 2 travelling between the columns 0 and 1, a second pair of traces will be connected to rows 1 and 2 of column 2 with the trace connected to row 2 extending between columns 2 and 3 and a third pair of traces which pass between columns 1 and 2 and are connected to the third row in each of these columns. In the event the technology permits more than two traces to be passed between a pair of adjacent rows, the above manner of connection would be altered, as is apparent.

It should be understood that, though the above described circuit has been laid out to accommodate differential pairs, each trace of each differential pair can be used to accommodate other types of signals.

It should be understood that the above described layout of signal traces can also be provided wherein the ball grid array is disposed on the same surface as the as the signal trace layout with the vias being eliminated, similar to the embodiment of FIGURE 3 and in the above referenced copending application but with the additional column and connections thereto as in the subject specification.

Advantages of the layout in accordance with the present invention are: improved electrical performance, suitability for high frequency applications and flexibility to use nearly all signal traces as differential pairs or single ended lines. Crosstalk is also substantially reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a schematic diagram of a typical package which can be used in accordance with the prior art as well as in accordance with the present invention;

FIGURE 2 is a cross sectional view of a portion of the package of FIGURE 1 connected to a printed wiring board;

FIGURE 3 is a schematic diagram of a layout in accordance with the present invention; and

FIGURE 4 is a preferred layout using three rows of vias for connection to the chip and a pair of traces between each pair of columns of vias.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIGURE 1, there is shown a typical package which can be used in accordance with the prior art as well as in accordance with the present invention. The package is shown with the encapsulation removed and includes a substrate 1 having a depression 3 which contains a chip 5. Bond wires 7 couple bond pads 8 on the chip 5 to individual copper traces 9 on the substrate, the copper traces each extending to an electrically conductive aperture or via 11 which extends through the substrate to a solder ball pad 12 and solder ball 13 as shown in FIGURE 2. The vias 11 and solder pad 12 are formed in a matrix array, there being plural rows and columns of vias which can be located adjacent one or more of the sides defining the depression 3. The solder ball 13 is soldered to a pad 15 on the printed wiring board 17 in standard manner as discussed in the above noted copending application to make the connection from the chip 5 to the printed wiring board terminal. While the traces 9 are shown on only one layer, it should be understood that there can be plural layers of signal traces separated by electrically insulating layers with vias extending from the top or interior layer of the substrate to the lower layer which contains ball pads and may also contain circuitry for additional electrical connections from the chip through substrate circuitry to the solder balls connected to the printed wiring board.. It should be understood that the above described layout of signal traces and substrate circuitry may also be inverted in a "cavity-down" configuration such that the solder balls are connected to the same side of the substrate as the chip.

The copper trace 9 as well as the bond wires 7, electrically conductive region in the via 11 and surrounding wiring add additional circuitry to the electrical circuit which bring to the circuit additional resistances, inductances and capacitances. The layout of the circuitry and especially the

traces 9 materially affect the performance of the chip, this being particularly material in the case of differential wiring pairs wherein pairs of wires carry the same or similar signals but are out of phase with each other. In accordance with the present invention, the path traversed by each trace 9 of each differential wiring pair is adjusted to have a pitch or distance therebetween from trace center line to trace center line of up to one solder ball 13 pitch, to be parallel to each for the maximum possible distance, to each be as close as possible to the same length and to have the same cross-sectional geometry to the closest extent possible. The pitch of the solder ball is set by the industry for the size of the package being used and varies, depending upon package size. In other words, it is a requirement that the parallel positioning of the trace portion of each differential wiring pair be maximized to the greatest possible extent and that the trace lengths be equalized to the greatest possible extent. The quality of the differential pairs is dependent upon each of (1) the degree of parallelism, (2) equality of length and (3) identity of cross-sectional geometry and spacing between the two traces forming the differential pair. It is also necessary that each trace of a differential pair be equally spaced from the ground plane.

In the present state of the art, it is possible to provide at most two signal traces between a pair of adjacent rows at minimum ball pitch. In order to meet the above criteria, it has been found that the above described maximization is obtained by connecting pairs in the manner 1-2, 1-2 and 3-3 as shown in FIGURES 3 and 4. In the event more or less than two traces can be or are passed between a pair of adjacent rows, the above manner of connection would be altered as is apparent.

It should be understood that, though the above described circuit has been laid out to accommodate differential pairs, each trace of each differential pair can be used to accommodate other types of signals.

Though the invention has been described with respect to a specific preferred embodiment thereof, many variations and modifications will immediately become apparent to those skilled in the art. It is therefore the intention that the appended claims be interpreted as broadly as possible in view of the prior art to include all such variations and modifications.

CLAIMS

1. A method of laying out traces for connection of bond pads of a semiconductor chip to a ball grid array printed wiring board substrate or the like which comprises the steps of:

(a) providing a substrate having a surface with a plurality of rows and columns of ball pads and having a solder ball secured to said ball pads; and

(b) providing a plurality of pairs of traces on said surface, each trace of each of said pairs of traces extending to a different one of said ball pads and extending to ball pads on a plurality of said rows and columns, each trace of each of said pair of traces being spaced from the other trace of said pair by up to a ball pitch, being maximized for identity in length and having up to one ball pitch difference in length and being maximized for parallelism and spacing.

2. The method of claim 1 wherein each of said traces of said pair is further maximized for identity in cross-sectional geometry.

3. The method of claim 1 further comprising the step of applying a differential signal pair to at least one of a said pair of traces.

4. The method of claim 2 further comprising the step of applying a differential signal pair to at least one of a said pair of traces.

5. The method of claim 1 further including the step of providing a further surface insulated from said surface, a plurality of said traces being disposed on said further surface.

6. The method of claim 2 further including the step of providing a further surface insulated from said surface, a plurality of said traces being disposed on said further surface.

7. The method of claim 3 further including the step of providing a further surface insulated from said surfaces, a plurality of said traces being disposed on said further surface.

8. The method of claim 4 further including the step of providing a further surface insulated from said surface, a plurality of said traces being disposed on said further surface.

9. A layout of traces for connection of bond pads of a semiconductor chip to a ball grid array printed wiring board substrate or the like which comprises:

(a) a substrate having a surface with a plurality of rows and colums of ball pads and having a solder ball secured to said ball pads; and

(b) a plurality of pairs of traces on said surface, each trace of each of said pairs of traces extending to a different one of said ball pads and extending to ball pads on a plurality of said rows and columns, each trace of each of said pair of traces being spaced from the other trace of said pair by up to a ball pitch, being maximized for identity in length and having up to one ball pitch difference in length and being maximized for parallelism and spacing.

10. The layout of claim 9 wherein each of said traces of said pair is further maximized for identity in cross-sectional geometry.

11. The layout of claim 9 further including means for applying a differential signal pair to at least one of a said pair of traces.

12. The layout of claim 10 further including means for applying a differential signal pair to at least one of a said pair of traces.

13. The layout of claim 9 further including a further surface between said top and bottom surfaces insulated from said top and bottom surfaces, a plurality of said traces being disposed on said further surface.

14. The layout of claim 10 further including a further surface insulated from said surface, a plurality of said traces being disposed on said further surface.

15. The layout of claim 11 further including a further surface insulated from said surface, a plurality of said traces being disposed on said further surface.

16. The layout of claim 12 further including a further surface insulated from said surface, a plurality of said traces being disposed on said further surface.

17. The method of claim 1 wherein said substrate has at least first, second and third rows and first, second, third and fourth columns of said ball pads in a matrix array, a first trace of a first pair of said traces extending to a ball pad in said first row of said second column closest to said chip and a second trace of said first pair of traces extending to a ball pad in said second row of said second column and between said first column and second column which is adjacent to said first column, a first trace of a second pair of said traces extending to a ball pad in said first row of said third column closest to said chip and a second trace of said second pair of traces extending to a ball pad in said second row of said third column and between said third column and said fourth column

which is adjacent to said third column, and first and second traces of a third pair of said traces extending to ball pads in said third row of said second and third columns and disposed between said second and third columns.

18. The layout of claim 9 wherein said substrate has at least first, second and third rows and first, second, third and fourth columns of said ball pads in a matrix array, a first trace of a first pair of said traces extending to a ball pad in said first row of said second column closest to said chip and a second trace of said first pair of traces extending to a ball pad in said second row of said second column and between said first column and second column which is adjacent to said first column, a first trace of a second pair of said traces extending to a ball pad in said first row of said third column closest to said chip and a second trace of said second pair of traces extending to a ball pad in said second row of said third column and between said third column and said fourth column which is adjacent to said third column, and first and second traces of a third pair of said traces extending to ball pads in said third row of said second and third columns and disposed between said second and third columns.

ABSTRACT OF THE DISCLOSURE

A method of laying out traces for connection of bond pads of a semiconductor chip to a printed wiring board or the like and the layout. There is provided a substrate having top and bottom surfaces with a plurality of rows and columns of vias extending therethrough from the top surface to the bottom surface and having a solder ball secured at the bottom surface to each via. A plurality of pairs of traces is provided on the top surface, each trace of each pair of traces extending to a different one of the vias and extending to vias on a plurality of the rows and columns, each of the traces of each pair being spaced from the other trace by a ball pitch, being maximized for identity in length and being maximized for parallelism and spacing. Each of the traces of a pair is preferably be further maximized for identity in cross-sectional geometry. A differential signal pair is preferably applied to at least one of a pair of traces. The layout can further include a further surface between the top and bottom surfaces insulated from the top and bottom surfaces, a plurality of the traces being disposed on the further surface.

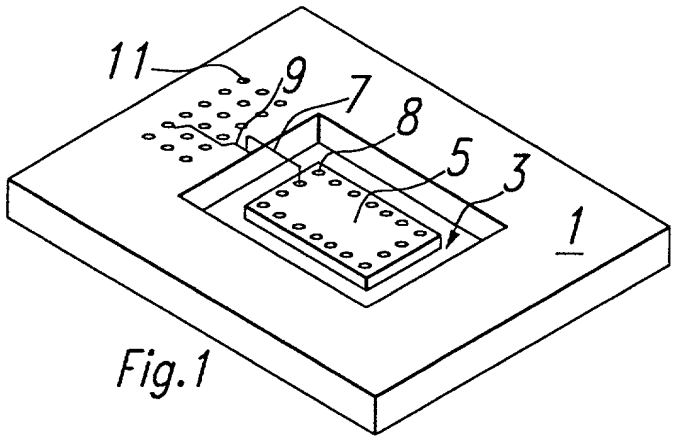

Fig.1

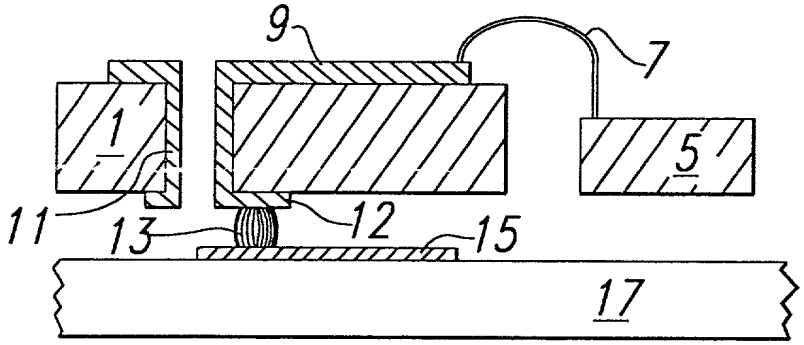

Fig.2

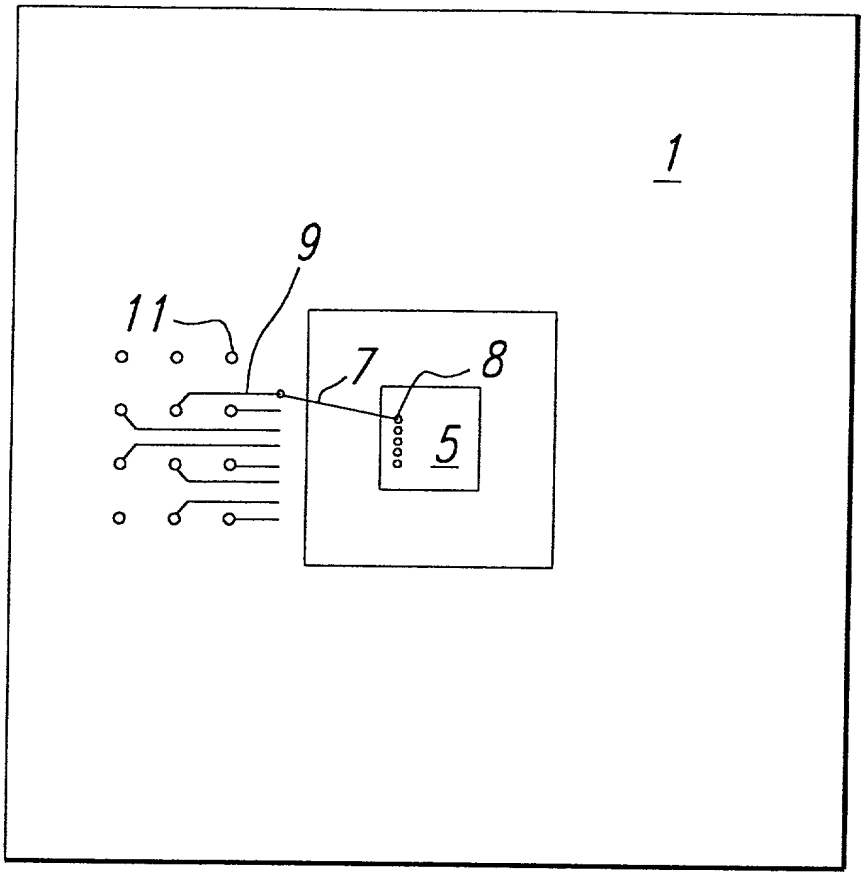

Fig.3

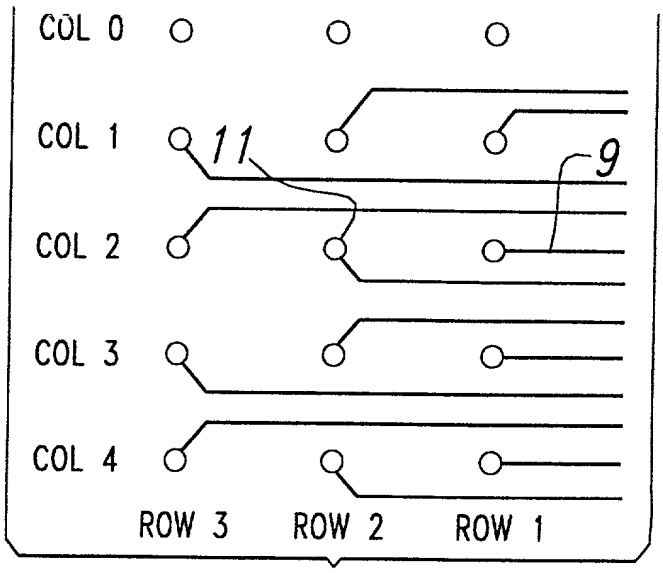

Fig.4

ATTORNEY'S DOCKET NO.
TI-25833

APPLICATION FOR UNITED STATES PATENT

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, section 1.56;

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION: OPTIMIZED CIRCUIT DESIGN LAYOUT FOR HIGH PERFORMANCE BALL GRID ARRAY PACKAGES		
POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH **Wade James Brady III, Reg. No. 32,080; Mark E. Courtney, Reg. No. 36,491; Alan K. Stewart, Reg. No. 35,373; Jacqueline J. Garner, Reg. No. 36,144; Jay M. Cantor, Reg. No. 19,906; William B. Kempler, Reg. No. 28,228; Richard L. Donaldson, Reg. No. 25,673**		
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Post Office Address **1517 Flintwood Dr.** **Richardson, TX 75081**	Post Office Address **3913 Windford Dr.** **Plano, TX 75023**	Post Office Address
COUNTRY OF CITIZENSHIP: **USA**	COUNTRY OF CITIZENSHIP: **USA**	COUNTRY OF CITIZENSHIP:
SIGNATURE OF INVENTOR: X	SIGNATURE OF INVENTOR: X	SIGNATURE OF INVENTOR:
DATE: X 3-02-98	DATE: X 03-01-98	DATE: